



Description

JBR5981 is a low-power isolated flyback converter. It operates at wide range of V_{IN} from 2.7V to 42V, and delivers up to 6W without the use of either additional transformer winding or opto-coupler. While the output voltage can be adjusted through a single external resistor, regulation is achieved through the feedback voltage in the primary-side. Further, the built-in soft-start, compensation, and 65V / 1.2A power switch of DMOS type make it possible for the external component count in the application circuit to be much reduced.

To achieve the best possible power efficiency without trading off performance, 3 operation modes (boundary, discontinuous conduction, low-ripple burst) are supported to achieve excellent load regulation and power efficiency across all loading condition.

JBZ8301 is manufactured [halogen, lead, antimony] free and RoHS compliant. Package offered is the low-profile SMT-type SOT-23-5L.

Applications

- Isolated power supply in end system where the line voltage is less than 42V
- Provisioning of isolated low voltage power supply (e.g. 5V, 3.3V) to instruments connected to serial buses like USB, CAN which are prevalent in industrial market and automotive after-market
- Auxiliary or housekeeping voltage supply in end terminals for industrial, telecommunication, networking, medical, and automotive applications

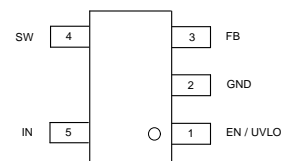
Features and Benefits

- Wide range of input voltages at 2.7 ~ 42V
- Integrated DMOS-Switch of 65V / 1.2A rating
- Low quiescent current: 145 μ A @ Sw. OFF; 350 μ A @ Sw. ON
- Boundary mode for heavy load, discontinuous conduction mode for medium load, burst mode for light load
- Load can be as little as 0.5% (typical) of full output
- Output voltage level is set via a single external resistor
- Neither 3rd transformer winding nor opto-isolator is needed for the regulation of output voltage
- Built-in soft-start and compensation to minimize external component count
- Integrated output short-circuit and over-temperature protection
- Lead-free SOT-23-5L assembled with 'green' molding compound

Pin Assignment

SOT-23-5L

(Top View)



Ordering Information

JBZ8301 S5

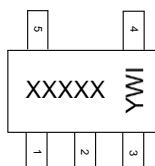
S5: SOT-23-5L

Product Name	Package	Marking	MSL	T _J (°C)	Media	Quantity (pcs)
JBZ8301S5	SOT-23-5L	J8301	3	-40 ~ 125	7" T&R	3,000

Marking Information

SOT-23-5L

(Top View)

First Line: Marking (see *Ordering Information*)

4 3

Second Line: Date Code

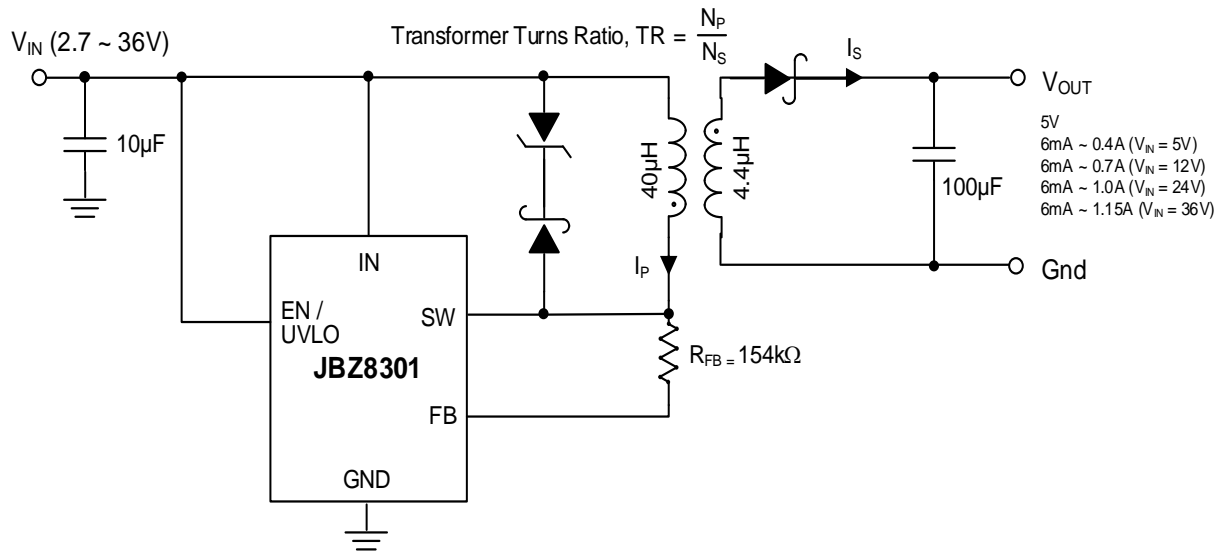
Y: Year of Molding

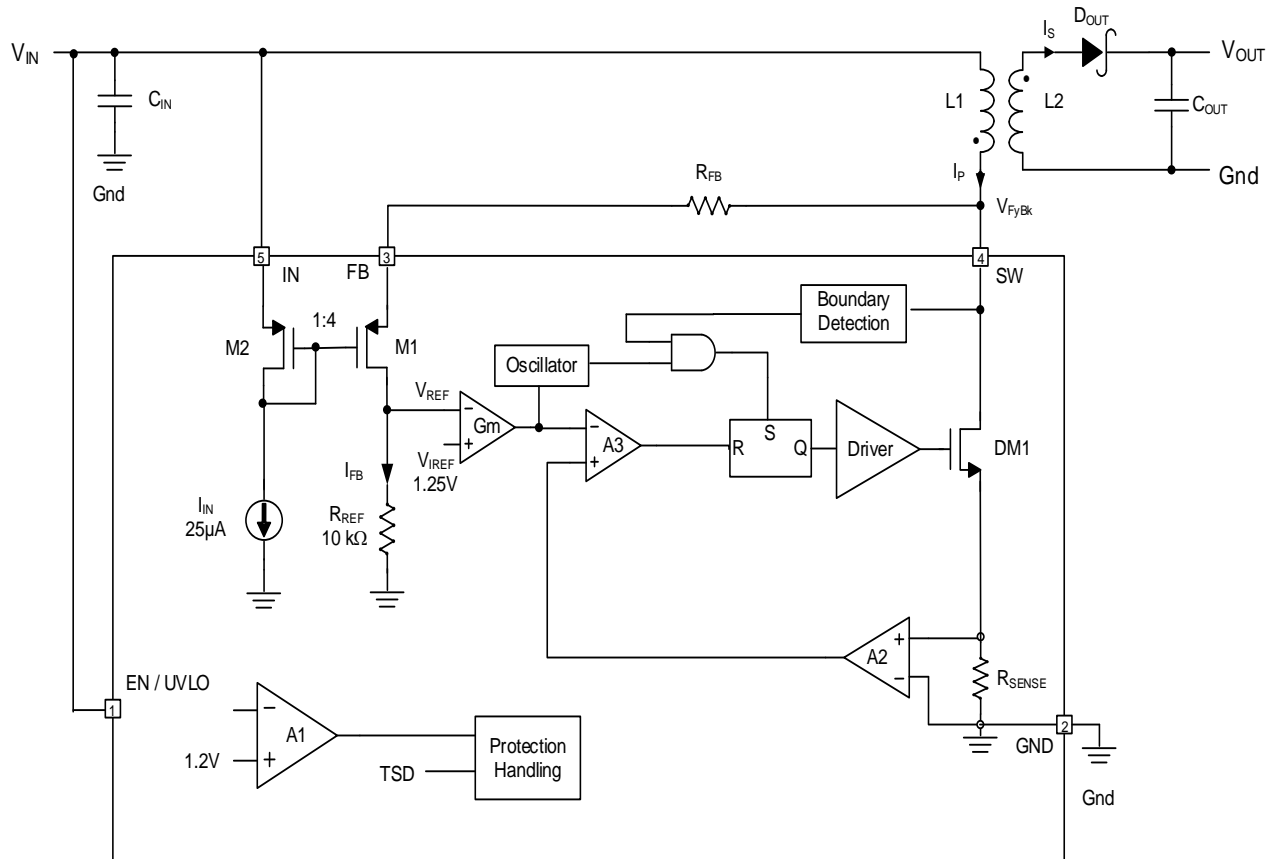
W: Work-week of Molding

I: Internal Code

Pin Description

Pin #	Pin Name	Type	Function
1	EN / UVLO	I	Enable / Under-voltage Lock-out. This is primarily used to turn ON or OFF the device, with the threshold preset at 1.2V. An external resistor divider can be used to program the UVLO threshold value. It can also be tied to V_{IN} directly.
2	GND	-	Device Ground. This is the ground reference for the device. It should be carefully connected to the ground plane with copper trace(s) and via(s) wherever appropriate.
3	FB	I	Feedback. It is connected to the SW pin and the positive voltage end of the transformer's primary winding. Ratio of R_{FB} to an internal resistor of $10k\Omega$ shall determine the output voltage.
4	SW	O	Switching Terminal: This is the Drain terminal of the internal DMOS-Switch (65V / 1.2A). Copper trace length to this pin on p.c.b. should be minimized to reduce EMI and unwanted voltage spikes.
5	IN	-	Supply Voltage. This pin supplies the power necessary for the device to operate properly and serves as reference for the feedback circuit associated to the FB pin. It should be connected with thick copper trace to a stable voltage source. A decoupling capacitor connected to GND helps to stabilize the input voltage level.

Typical Application Circuit

Fig. 1: Application Circuit

Functional Blocks

Fig. 2: Diagram of Internal Functional Blocks
Absolute Maximum Ratings (All measurements were made at $T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	-	-	42	V
V_{SW}	Voltage at Drain terminal of Internal 65V DMOS-Switch ¹	-	-	65	V
$V_{EN/UVLO}$	Voltage at EN / UVLO Pin	-	-	V_{IN}	V
V_{FB}	Voltage at FB Pin	$V_{IN} - 0.5$	-	V_{IN}	V
I_{FB}	Current into FB Pin	-	-	200	μA
T_J	Junction Temperature	-40	-	125	$^\circ\text{C}$
T_{STG}	Storage Temperature	-65	-	150	$^\circ\text{C}$

Note 1: SW pin is rated to 65V for spurious voltage spikes. In order to keep the SW pin operating reliably, it is best to de-rate the flyback voltage spike to less than 65V.

**Recommended Operating Conditions** (All measurements were made at $T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input Voltage	2.7	42	V
T_J	Operating Junction Temperature	-40	150	$^\circ\text{C}$

Electrical CharacteristicsTest Conditions [$V_{IN} = 12\text{V}$; $T_A = 25^\circ\text{C}$] are applicable to the following measurement unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage Range	-	2.7	-	42.0	V
	UVLO Threshold for V_{IN}	Rising	-	2.55	2.65	
		Declining	2.25	2.35	-	
I_Q	Quiescent Current	$V_{EN/UVLO} = 0\text{V}$	-	1	3	μA
		Sleep Mode (DMOS-Switch OFF)	-	145	190	
		Active Mode (DMOS-Switch ON)	-	350	460	
V_{EN}	Threshold for Device Enable	Rising	-	1.2	1.3	V
		Declining	1.0	1.1	-	V
I_Q	Quiescent Current	$V_{EN/UVLO} = 0\text{V}$	-	1	3	μA
		Sleep Mode (DMOS-Switch ON)	-	145	190	
		Active Mode (DMOS-Switch OFF)	-	350	460	
f_{SW_Min}	Minimum Switching Frequency	-	8	10	12	kHz
t_{ON_Min}	Minimum DMOS-Switch ON Time	-	-	160	-	ns
t_{OFF_Min}	Minimum DMOS-Switch OFF Time	-	-	450	-	ns
t_{OFF_Max}	Maximum DMOS-Switch OFF Time	-	-	190	-	μs
I_{SW_Min}	Minimum Switched Current	-	0.29	0.39	0.49	A
I_{SW_Max}	Maximum Switched Current	-	-	1.5	-	A
I_{LKG}	Leakage Current of DMOS-Switch	$V_{IN} = 42\text{V}; V_{SW} = 65\text{V}$	-	-	2	μA
I_{FB}	Regulation Current at FB Pin	-	96	100	104	μA
	Line Regulation	$2.7\text{V} < V_{IN} < 42\text{V}$	-	-	0.1	%/V
$R_{DS(ON)}$	ON Resistance of DMOS-Switch	$I_{SW} = 500\text{mA}$	-	390	-	$\text{m}\Omega$
T_{TSD}	Thermal Shut-down Threshold	-	-	150	-	$^\circ\text{C}$
	Thermal Shut-down Hysteresis	-	-	20	-	$^\circ\text{C}$

Thermal Properties

Test Conditions: Device mounted on FR-4 substrate, 2-layer PCB, 2oz copper, with minimum recommended cooling pad to dissipate heat

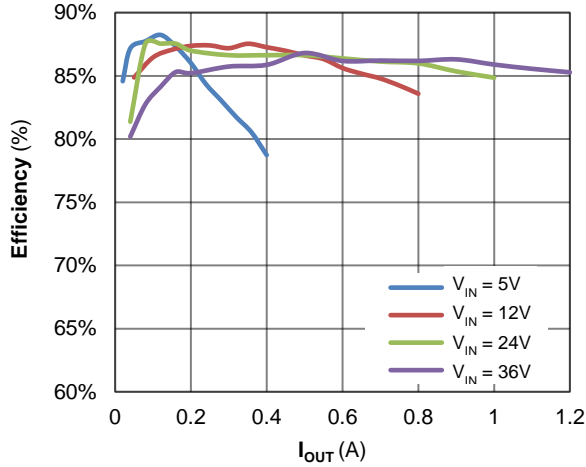
Symbol	Parameter	Conditions	Rating	Unit
$R_{\theta JA}$	Thermal Resistance (junction-to-ambient)	SOT-23-5L	162	$^\circ\text{C}/\text{W}$



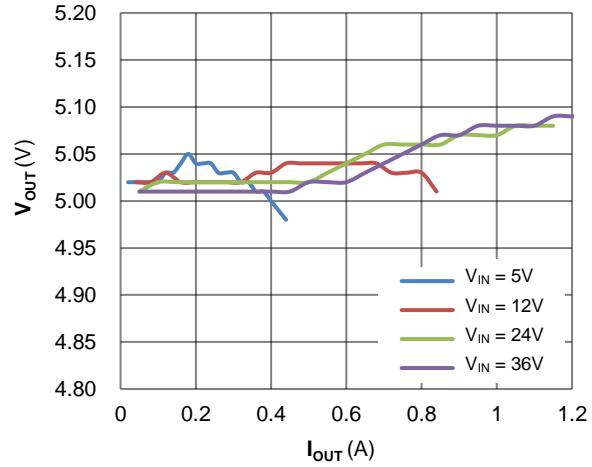
Typical Performance Characteristics

Unless otherwise stated, the following test conditions apply: $T_A = 25^\circ\text{C}$

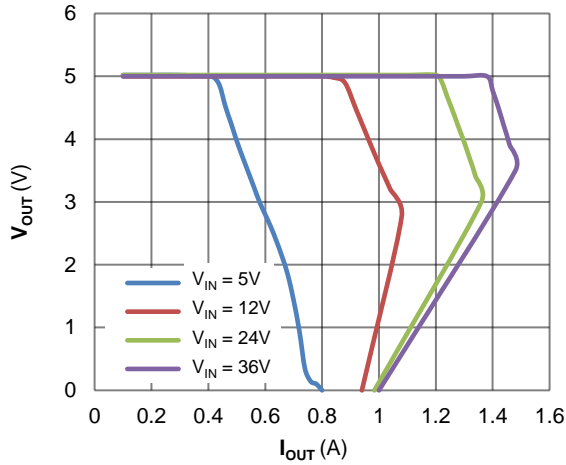
Graph 1: Efficiency vs. Load Current



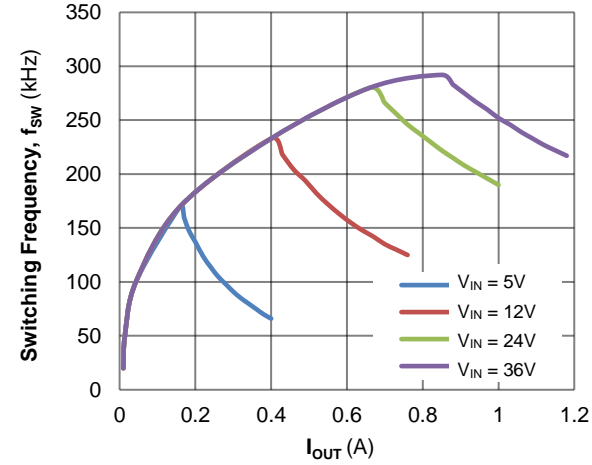
Graph 2: Output Load and Line Regulation



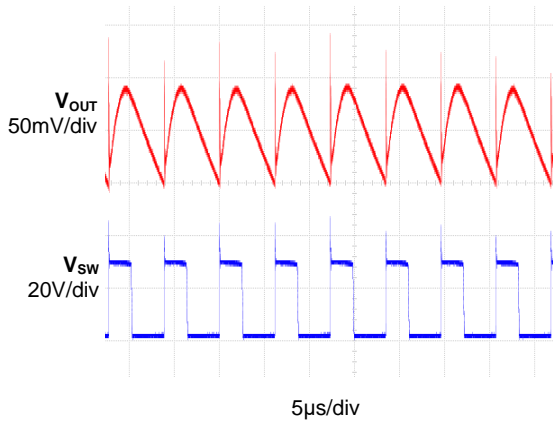
Graph 3: Output Short-Circuit Protection



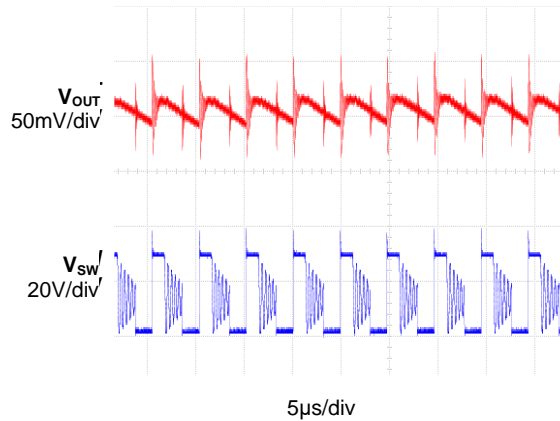
Graph 4: Switching Frequency vs. Load Current



Graph 5: Boundary-mode Waveforms ($V_{IN} = 12\text{V}$; $I_{OUT} = 600\text{mA}$)



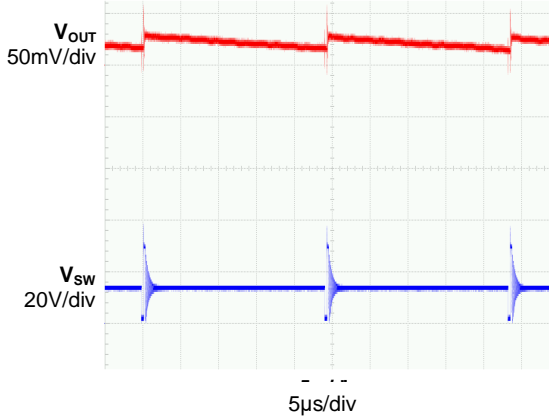
Graph 6: Discontinuous-mode Waveforms ($V_{IN} = 12\text{V}$; $I_{OUT} = 600\text{mA}$)



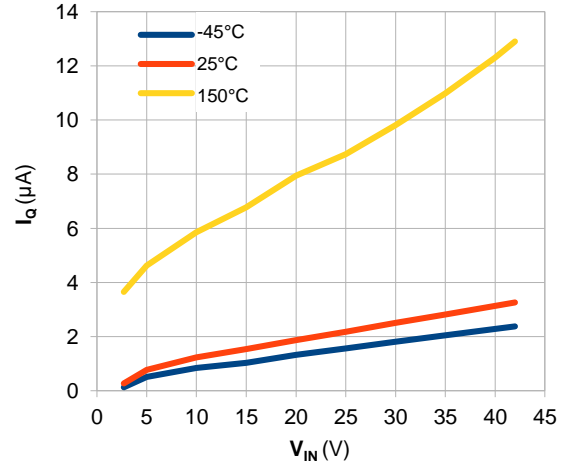
Typical Performance Characteristics (Continued)

Unless otherwise stated, the following test conditions apply: $T_A = 25^\circ\text{C}$

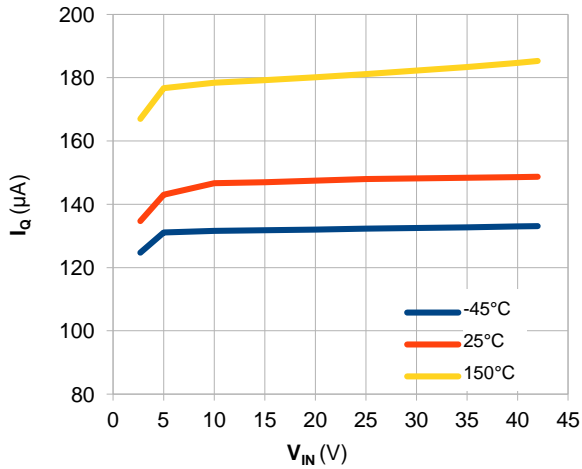
Graph 7: Burst-mode Waveforms ($V_{IN} = 12\text{V}$; $I_{OUT} = 600\text{mA}$)



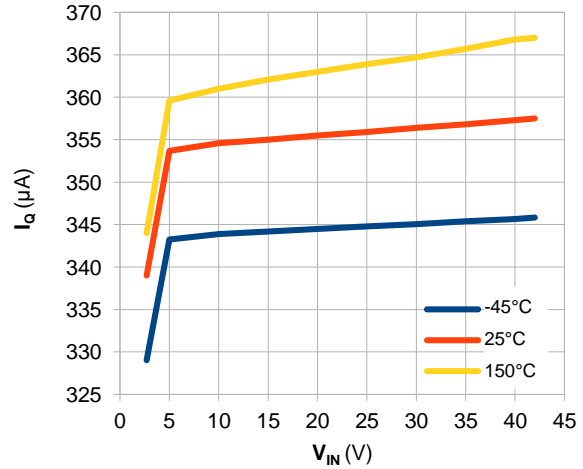
Graph 8: Shutdown Current vs. V_{IN}



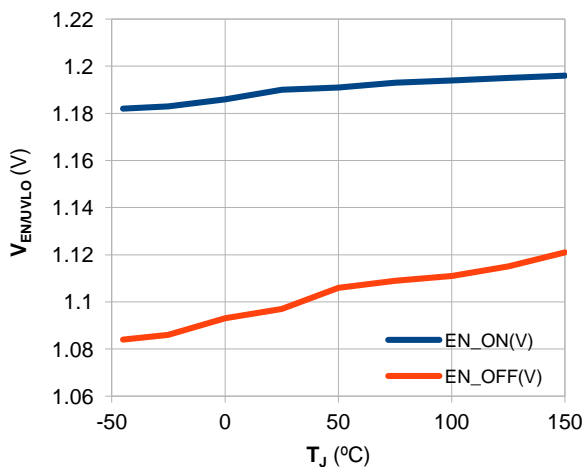
Graph 9: Quiescent Current @ Sleep Mode vs. V_{IN}



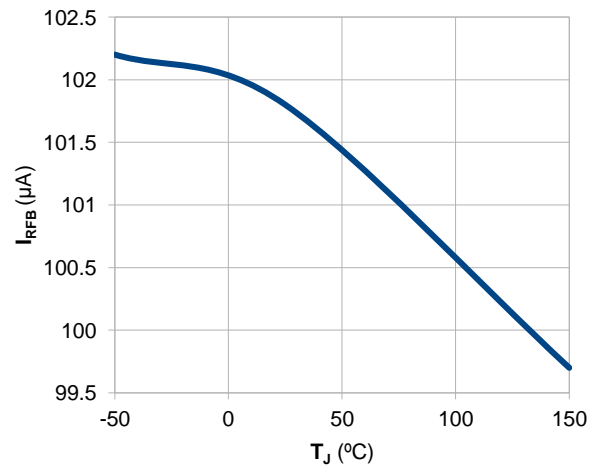
Graph 10: Quiescent Current @ Active Mode vs. V_{IN}



Graph 11: EN/UVLO Enable Threshold vs. T_A



Graph 12: R_{FB} Regulation Current vs. T_A

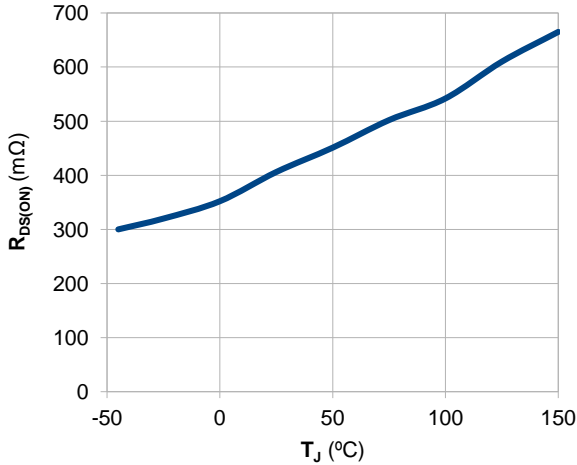




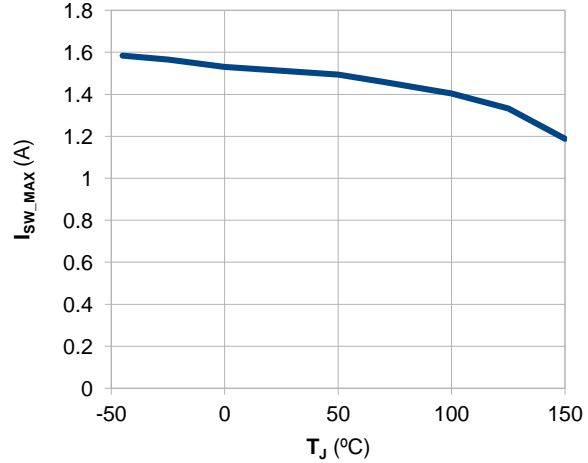
Typical Performance Characteristics (Continued)

Unless otherwise stated, the following test conditions apply: $T_A = 25^\circ\text{C}$

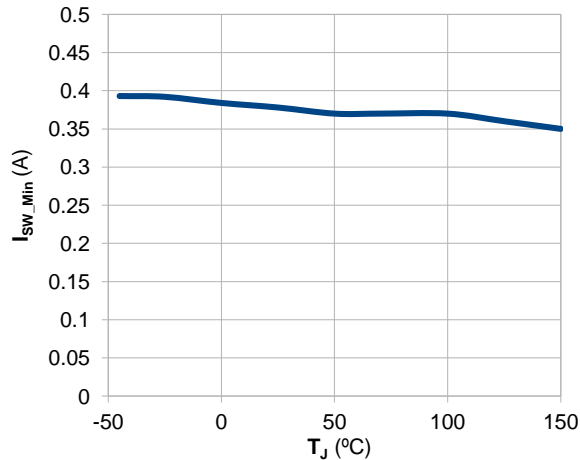
Graph 13: $R_{DS(ON)}$ vs. T_A



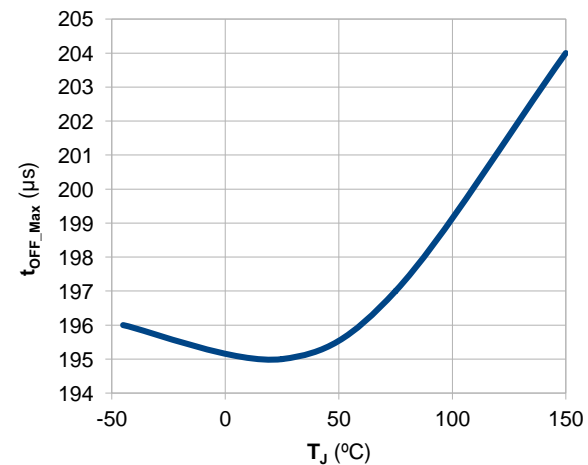
Graph 14: Maximum Switched Current Limit vs. T_A



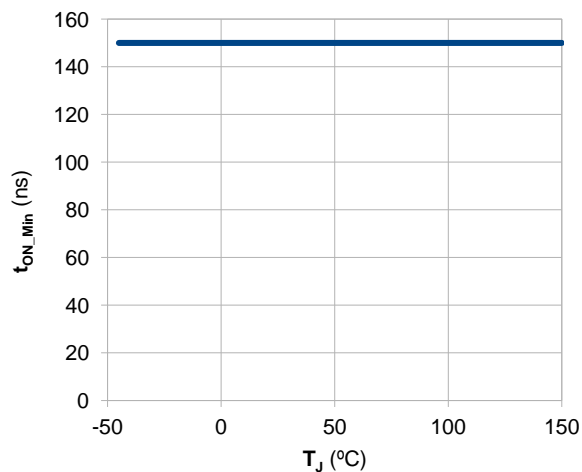
Graph 15: Minimum Switch Current Limit vs. T_A



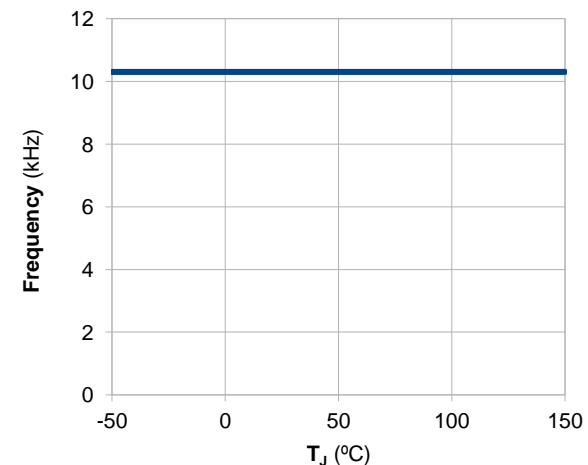
Graph 16: Maximum DMOS-Switch OFF Time vs. T_A



Graph 17: Minimum DMOS-Switch ON Time vs. T_A



Graph 18: Minimum Switching Frequency vs. T_A





Detailed Description of Device Operation

Overview

JBZ8301 is a current-mode isolated fly-back switching converter with integrated 60V DMOS-Switch. The novel flyback pulse-sense circuit samples the isolated output voltage through the primary-side flyback pulse waveform. Neither opto-coupler nor additional transformer windings to achieve regulation in the isolated flyback topology is needed. As a result, the disadvantages caused by the opto-coupler like [wasted output power, limited dynamic response, nonlinearity, uneven aging of the individual components within] and the extra windings like mediocre dynamic response, power deficiency, increased physical size and cost] no longer exist.

In order to reduce the number of external components necessary for proper operation, the following functions are integrated: voltage reference, oscillator logic, current amplifier & comparator, sample-&-hold error amplifier, 60V DMOS power switch, loop compensation, soft-start. For exception handling, short-circuit protection and over-temperature shut-down are implemented. To meet regulatory requirement for power efficiency, under heavy to medium load, boundary conduction mode and discontinuous conduction mode are activated such that the output voltage is always sampled on the SW pin whenever the current in the secondary-side becomes 'zero'. As such, the load regulation is improved without the need for external load compensation components. To further improve the power efficiency at light load, low-ripple burst mode is supported.

Boundary Conduction Mode

This mode of operation, in practice a variable frequency & peak-current switching scheme, facilitates optimum power efficiency at heavy load. Because the current in the secondary-side (I_s) always returns to 'zero' every cycle, the parasitic resistive voltage drop does not affect the load regulation performance. In addition, sub-harmonic oscillation practically does not exist. In contrast to the continuous conduction mode, smaller transformer size becomes feasible.

When the current (flowing through the output diode), I_s , in the secondary-side reaches 'zero', the internal DMOS-Switch shall be turned ON. Subsequently, the current (I_p) in the primary-side of the transformer increases until a pre-set current limit is reached. Once the DMOS-Switch is turned OFF, V_{SW} rises to approximately $(V_{OUT} \times TR) + V_{IN}$. When the current in the secondary-side (I_s) falls to zero again, V_{SW} collapses and rings round V_{IN} . At that time, the internal "boundary mode detector" shall be triggered and subsequently turns ON the internal DMOS-Switch, DM1.

Discontinuous Conduction Mode

When the load on the secondary-side becomes lighter, the Boundary Conduction Mode shall increase the switching frequency (f_{SW}) to a maximum value of 400kHz. At that time, the turn-ON time of the DMOS-Switch is also delayed. In comparison to the Boundary Conduction Mode, the Discontinuous Conduction Mode results in reduced switching loss and gate charge loss.

Low-ripple Burst Mode

Quite unlike the typical implementation of flyback converters, JBZ8301 must keep turning ON & OFF the internal DMOS-Switch for a minimum amount of time and at a minimum f_{SW} of 10kHz (typical value). In addition, the minimum switched current limit (I_{SW_Min}) and the minimum switch-OFF time must be maintained for proper operation of the internal circuitries.

Under the Low-ripple Burst Mode of operation, the JBZ8301 practically alternates between the sleep and active states. The output voltage is sampled at the minimum switching frequency of 10kHz (typical), effectively reducing the quiescent current hence improved power efficiency under the light load condition.



Application Information

Setting Output Voltage

The JBZ8301 operates similarly to a typical DC-DC buck converter with one exception. The combination of the built-in flyback pulse sense circuit and sample-&-hold error amplifier samples the flyback pulse and subsequently regulates the isolated V_{OUT} . In this operation, the feedback resistor (R_{FB}) is used to set the output voltage, V_{OUT} .

Once the internal DMOS-Switch is turned OFF, V_{SW} rises above V_{IN} . The voltage difference, i.e. amplitude of the flyback pulse, can be calculated by the formula shown below:

$$V_{FyBk} = \{[V_{OUT} + V_F + (I_S * ESR)] * TR\}; \text{ where,}$$

V_F = Forward Voltage over Output Diode
 I_S = Current in Secondary-side of Transformer
 ESR = Total Impedance of Transformer's Secondary-side Windings
 TR = Effective Primary-to-Secondary Turns Ratio of Transformer = N_P / N_S

The built-in flyback pulse sense circuit (M1 & M2) subsequently generates I_{FB} from the V_{FyBk} , which is then converted to V_{REF} after passing through the internal resistor R_{REF} (10k Ω). Because the sample-&-hold error amplifier only samples V_{REF} when I_S in the secondary-side becomes 'zero', the multiplication of $[I_S * ESR]$ shall result in zero value. The closed feedback loop eventually causes $V_{REF} \cong V_{IREF}$ (an internally generated reference voltage at 1.25V) hence the resultant relationship between V_{FyBk} and V_{IREF} can be represented by the formula shown below:

$$(V_{FyBk} / R_{FB}) * R_{REF} = V_{IREF} \rightarrow$$

$$V_{FyBk} = (V_{IREF} / R_{REF}) * R_{FB} \rightarrow$$

$$V_{FyBk} = I_{FB} * R_{FB}; \text{ where}$$

$V_{REF} \cong V_{IREF}$
 I_{FB} = Regulation Current over $R_{FB} \cong 100\mu A$

Combing these two formulae for V_{FyBk} would yield the formula shown below:

$$V_{OUT} = (I_{FB} * (R_{FB} / TR) - V_F); \text{ where } I_{FB} \cong 100\mu A$$

Output Temperature Coefficient

In the formula used to calculate V_{FyBk} in the last section, the negative temperature coefficient typically associated to the output diode necessary for the proper operation of the transformer's secondary-side is not considered. Such negative temperature coefficient (typically from -1mV/ $^{\circ}C$ to -2mV/ $^{\circ}C$) can produce approximately 200mV to 300mV variation over V_F hence V_{OUT} across temperatures.

At higher levels of V_{OUT} , for example 12V & 24V, the negative temperature coefficient likely does not adversely affect the output voltage regulation. However, at low levels of V_{OUT} like 3.3V and 5V, the negative temperature coefficient of the output diode can count for an additional 2 ~ 5% of output voltage regulation.

Selection Criteria for Value of Feedback Resistor, R_{FB}

The JBZ8301 employs a novice approach (sampling scheme) to regulate V_{OUT} , in which repeatable delays and error sources are involved. As such, a two-step process to adjust the value of R_{FB} must be implemented.

$$R_{FB_Initial} = [TR * (V_{OUT} + V_F) / I_{FB}]; \text{ where}$$

$I_{FB} \cong 100\mu A$
 $V_F \cong 0.3V$

Step 1. Assuming an initial value, $R_{FB_Initial}$, calculated from the desired V_{IN} and V_{OUT} , the regulated output voltage is measured as V_{OUT_Mesrd} .

Step 2. Taking the formula shown at the end of the section *Setting Output Voltage*, a slight re-arrangement reveals the expression shown below. The actual value of the feedback resistor to be used shall be calculated from this formula.

$$R_{FB_Actual} = [(V_{OUT} / V_{OUT_Mesrd}) * R_{FB_Initial}]$$

Considering the parametric variation of all the external components used in the real-life application circuit, the accuracy of the output voltage regulation will typically be within $\pm 5\%$ typically. This projection further assumes resistor tolerances and matching of transformer windings within $\pm 1\%$.

Selection of Inductance in Primary-side

In the operation of the JBZ8301, conduction of the I_S in the secondary-side eventually results in the V_{OUT} being reflected at the SW pin in the primary-side. In order for the internal sample-&-hold circuit to capture the reflected- V_{OUT} correctly, I_S must stay conducted for 450ns at the very least. As such, the formula shown below gives the minimum value for the primary-side magnetizing inductance:



$$L_P \geq \{[t_{OFF_Min} * TR * (V_{OUT} + V_F)] / I_{SW_Min}\}; \text{ where } \begin{array}{l} t_{OFF_Min} = \text{Minimum DMOS-Switch OFF Time} = 450\text{ns} \\ I_{SW_Min} = \text{Minimum Switched Current in Primary-side} = 390\text{mA (typical)} \end{array}$$

In addition, whenever the internal DMOS-Switch is turned ON, it must remain ON for 160ns (typical) at the very least. This is the leading-edge blanking time during the power-up of the internal DMOS-Switch, in which the internal circuitries shall ignore the occurrence of any current spikes. Non-compliance likely results in oscillation at the output because the current control loop fails to regulate. Given these, the formula shown below shall be used to calculate the primary-side magnetizing inductance:

$$L_P \geq [(t_{ON_Min} * V_{IN_Max}) / I_{SW_Min}]; \text{ where } t_{ON_Min} = \text{Minimum DMOS-Switch ON Time} = 160\text{ns}$$

As a general rule of thumb, the primary magnetizing inductance of the transformer shall be ~ 30% larger than the minimum values calculated with the formulae shown above. Nonetheless, the larger the inductance, the bigger the physical size and the risk of instability under light load condition.

Turns Ratio

Through the use of feedback resistor (R_{FB}) to determine the output voltage (V_{OUT}), system engineers have high degree of freedom to choose the turns ratio (TR) of the transformer necessary for JBZ8301 application circuit to operate properly. In practice, simple ratios of small integers like 3:1, 2:1, 1:1 facilitate the different combination of total turns and mutual inductance. As the value of TR affects the V_{OUT} accuracy, transformer with TR Accuracy of $\pm 1\%$ is recommended for the reliable operation of JBZ8301.

In general, TR is used to maximize the output power. At low output voltage levels like 3.3V or 5.0V, larger TR (N:1) can be used to maximize the current gain and output power of the transformer. Because the SW pin often sees a high voltage equal to $[V_{IN_Max} + (V_{OUT} * TR)]$ plus on-top a voltage spike (V_{LKG}) caused by leakage inductance, care must be taken to ensure that the internal DMOS-Switch is not stressed beyond its maximum rating of 65V. All these set the upper limit to the value of TR for a given application. As a rule of thumb, TR should be made low enough such that the condition shown below is always true.

$$TR < [(65V - V_{IN_Min} - V_{LKG}) / (V_{OUT} + V_F)]$$

For lower output power, a smaller TR relieves the stress upon the SW pin. Although a TR of 1:N can yield very high output voltage level without exceeding the breakdown voltage of the internal DMOS-Switch, the parasitic capacitance within the windings can cause the turn-ON spike of the DMOS-Switch to ring beyond the leading-edge blanking period, i.e. t_{ON_Min} of 160ns (typical). Consequently, instability under light load condition could occur hence the use of TR of 1:N shall always be carefully evaluated.

Saturation Current

In a typical transformer, once the core is saturated, energy injected into the core from the primary windings shall not be transferred to the secondary windings. Instead, the energy are dissipated within the magnetic core. As such, care much be taken to ensure that the current in the transformer windings does not exceed the rated saturation current limit of the transformer.

Winding Resistance

Power efficiency is adversely affected by the resistance of the primary and secondary windings. In contrast, output voltage regulation is independent of the resistance of the windings. This is due to the effect of the boundary and discontinuous conduction modes of operation supported by the internal circuitries of the JBZ8301.

Under-voltage Lockout, UVLO

In accordance to the application circuit shown in Fig. 3, a resistive divider between the V_{IN} terminal and Gnd with the center tap connected to EN / UVLO pin allows the UVLO function to be realized. The JBZ8301 is enabled when the input voltage level at EN / UVLO pin rises above 1.2V with hysteresis of 100mV.

With the UVLO function enabled, external shut-down control can also be realized as shown in Fig. 3. Upon being turned ON, the external N-type MOSFET shall connect the EN / UVLO pin to Gnd hence the JBZ8301 is effectively shut down. The I_Q consumed shall be less than 3 μ A at the very most.

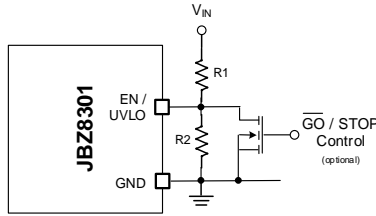


Fig. 3: Under-voltage Lock-out (UVLO) with External ON / OFF Switch

Minimum Load Requirement

In typical operation, the JBZ8301 samples the isolated V_{OUT} from the flyback pulse (V_{FyBk}) exists in the primary-side. The flyback pulse occurs whenever the internal DMOS-Switch in the primary-side is turned OFF and I_S in the secondary-side conducts. The internal DMOS-Switch has to be turned ON and OFF for a minimum amount of time and at a minimum switching frequency. Nonetheless, a minimum amount of energy is delivered by the JBZ8301 even under light load condition to ensure accurate output voltage. As such, delivery of the minimum energy results in *minimum load requirement* which can be expressed as below:

$$I_{LOAD_Min} = [(L_P * I_{SW_Min}^2 * f_{SW_Min}) / (2 * V_{OUT})]; \text{ where } L_P = \text{Inductance of Transformer's Primary Windings}$$

I_{SW_Min} = Minimum Switched Current = 490mA (maximum)
 f_{SW_Min} = minimum Switching Frequency = 12kHz (maximum)

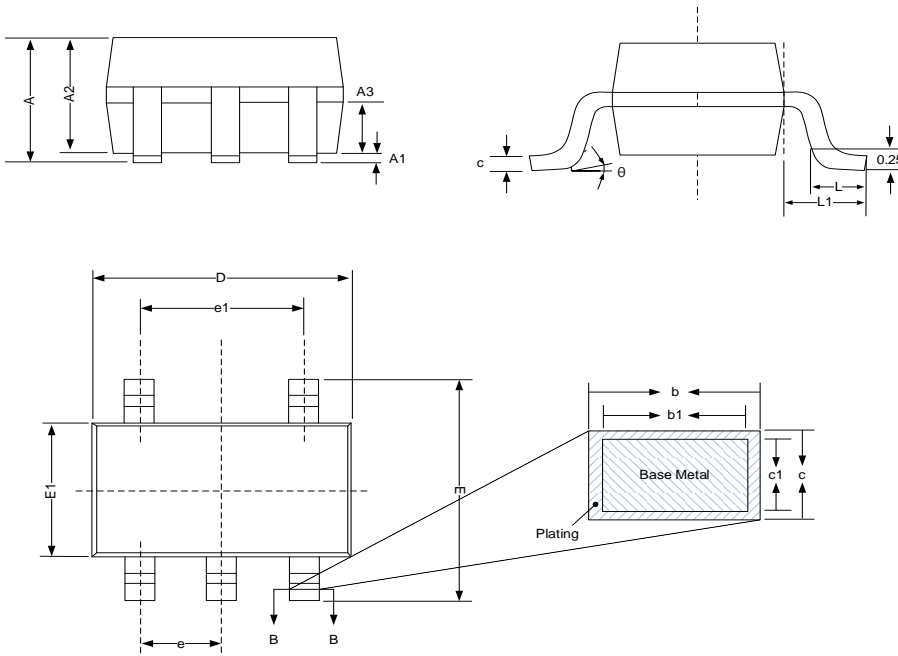
The JBZ8301 typically requires less than 0.5% of its full output power as the minimum load. As an alternative, a zener diode with its break-down voltage at 20% higher than the V_{OUT} of the application circuit of JBZ8301 can serve as a minimum load if pre-loading cannot be accepted. Assuming the desired V_{OUT} of 5V, a zener diode with break-down voltage at 6V should be connected between the V_{OUT} terminal and GND.

Short-circuit Protection at Output

When the output of the JBZ8301 application circuit is either heavily over-loaded or shorted, the voltage spikes reflected at the SW pin likely rings longer than the pre-set blanking time. After the blanking time expires and with no additional exception handling implemented, the *boundary* mode detector could be falsely triggered by the excessive rings. As a result, the internal DMOS-Switch is turned ON again well before the current (I_S) in the secondary-side falls to 'zero'. Subsequently, the JBZ8301 runs into *continuous conduction* mode at maximum switching frequency. All these cause the switched current (I_{SW}) to undergo *run away* condition. Nevertheless, once the JBZ8301 detects significant drop from regulation upon the output voltage, the internal control logics gradually reduces the switched current to the level below 1.5A (i.e. typical value of I_{SW_Max}).

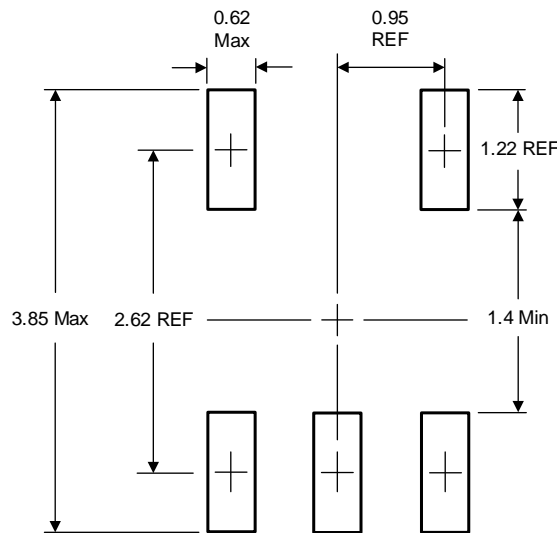
In the worst case situation where the output of the JBZ8301 application circuit is directly shorted to Gnd through a long wire, the huge rings after the temporary fold-back of the switched current and switching frequency likely still falsely triggers the *boundary* mode detector, the secondary over-current protection mechanism shall subsequently be activated. Once the switched current hits the internally-set hard limit of 2.2A, a soft-start cycle initiates. This results in a hard pull-back of both the switched current limit and switching frequency.

Package Outline (All measurements in mm)

Package Type: SOT-23-5L (J2)


SOT-23-5L (J2)			
Dimension	Min.	Typ.	Max.
A	-	-	1.25
A1	0.04	-	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.38	-	0.47
b1	0.37	0.40	0.43
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	-	0.60
L1	0.60 REF		
θ	0°	-	8°
All measurements in "mm"			

Suggested Pad Layout (All measurements in mm)

Package Type: SOT-23-5L (J2)

 Recommended Solder Pad Layout
(per IPC Stds.)



JBZ8301

42V Isolated Flyback Converter

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